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10/628,562	07/29/2003	Bi-Yun Yeh	SUND 114CIP	4818

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/628,562	YEH ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 09 February 2007.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6,12-27 and 32-34 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 and 12-27 is/are rejected.

7)☒ Claim(s) 32-34 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 29 July 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This final action is in response to communications filed on 2/9/07.

2. Claims 1, 12, 20, 32 33, 34 have been amended, claims 7-11, 28-31 have been canceled and no new claims have been added. Thus, claims 1-6, 12-27, 32-34 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 12-27 are rejected under 35 U.S.C. 103(a) as anticipated by Klein (US Patent 6216224), in view of Applicant's Admission of Prior Art (AAPA).

For claim 1, Klein teaches the following limitations:

A method for accessing initialization data (102 in Fig 1) **for starting a central processor unit** (lines 55-57 of column 3; lines 5-10 of column 1) **in a computer system** (Fig 1) **comprising:**

- **providing a non-volatile memory** (104) **connected to the south-bridge chip** (110), **wherein the non-volatile memory includes a first memory space storing routines and code of a basic input/output system (BIOS)**

and a second memory storing initialization data, and wherein the initialization data is excluded from the BIOS (lines 28-36 of column 1 mention that firmware routines include BIOS and various initialization routines. Lines 55-60 of column 1 mention that BIOS firmware is different from initialization routines. Since BIOS and initialization routines are different, they are saved in different space in firmware. Therefore, first memory space includes BIOS and second memory space includes initialization data) **and is used for initialization of the central processor unit** (line 56 of column 1 mentions that the routine is CPU initialization routine);

- **sending a request from the north-bridge chip to South bridge chip** (lines 25-30 of column 3 mention that the system controller 114 transfers ROM data 102 to RAM 118. Thus, the North Bridge 114 requests for initialization data 102 through South Bridge 110) **in order to access initialization data from the second memory space of non-volatile memory** (lines 20-35 of column 1);
- **starting up the central processor unit by receiving the initialization data sent from the south-bridge chip** (lines 7-12 of column 4 mention that CPU is activated after firmware transfers to RAM, which includes 114) **and then initializing the central processing unit based on the initialization data received by the north-bridge chip from the south bridge chip** (lines 1-20 of column 2).

Klein (US Patent 6216224) does not explicitly mention that 114 is the north bridge and 110 is the south bridge. Instead, 114 is labeled as system controller in line 7 of column 2 and 110 is labeled as ISA-PCI bridge in line 28 of column 4.

System controller and ISA-PCI bridge are known as north bridge and south bridge respectively. To support the statement, Examiner presents Klein (US Patent 5974239), which mentions that system controller is sometimes called the north bridge (lines 47-48 of column 1) and the bridge between PCI and ISA bus is called South bridge (lines 60-61 of column 1; lines 59-60 of column 4). Thus, Klein (US Patent 5974239) interchangeably used “system controller” with “north bridge” and “ISA bridge” with “south bridge”.

Klein does not teach setting initial values for initialization of the CPU based on received initialization data received by North bridge. Klein uses a random access memory to store initialization data.

applicant admits that the following limitations exist in prior art:

A method for accessing initialization data for starting a central processor unit in a computer system (Fig 1 and 2 show that the serial PROM 200 is storing initialization data for starting a central processing unit 208 in a computer system of Fig 1) **comprising:**

- **starting up a north-bridge chip** (line 20 of page 3) **that is coupled between CPU** (208) **and South bridge chip** (206);
- **requesting said initialization data by said north bridge chip** (lines 20-22 of page 3) **in order to access initialization data from a non-volatile memory** (200).
- **receiving said initialization data by said north-bridge chip** (lines 21-22 of page 3), **starting CPU for initialization of the CPU based on the received initialization data** ([0007] of page 3).
- **setting initialization values for initialization using the initialization data sent by the north bridge** (lines 20-27 of column 2).
- **No RAM to store initialization data** (Fig 2).

It would have been obvious to one ordinary skill in the art at the time the invention was made to have combined the teachings of Klein and AAPA. One ordinary skill in the art would have been motivated to set initial values for initialization of the CPU based on received initialization data from North Bridge, since that is a necessary step for initialization. One ordinary skill in the art would be motivated to omit the RAM as it is a faster way to initialize the CPU.

For claims 2, 3, lines 23-24 of page 2 of applicant's disclosure mention that the initialization data may include SIP data used in AMD CPUs.

For claim 4, note lines 19-21 of [0007] of page 3 of applicant's disclosure, which mention that the South Bridge is powered and starts up the North Bridge.

For claim 5, requesting includes sending a signal from north bridge chip (114) to South bridge chip (104).

For claim 6, lines 22-24 of [0007] of page 3 of applicant's disclosure mention that the CPU sets initial value using initialization data sent by North Bridge and operates normally. Thus, the method further comprises sending said initialization data to the central processor unit of said computer system for starting up the central processor unit.

For claim 12, Klein teaches the following limitations:

A method for accessing initialization data (102 in Fig 1) **for starting a central processor unit** (lines 55-57 of column 3; lines 5-10 of column 1) **in a computer system** (Fig 1) **that also includes a bus** (112), **a south bridge chip** (110) **connected to the bus, and a north bridge chip** (114) **connected between the bus** (112) **and the central processing unit** (106), **the method comprising:**

- **providing a non-volatile memory** (104) **connected to the south-bridge chip** (110), **wherein the non-volatile memory includes a first memory space storing routines and code of a basic input/output system (BIOS) and a second memory storing initialization data, and wherein the initialization data is excluded from the BIOS** (lines 28-36 of column 1 mention that firmware routines include BIOS and various initialization routines.

Lines 55-60 of column 1 mention that BIOS firmware is different from initialization routines. Since BIOS and initialization routines are different, they are saved in different space in firmware. Therefore, first memory space includes BIOS and second memory space includes initialization data) **and is used for initialization of the central processor unit** (line 56 of column 1 mentions that the routine is CPU initialization routine);

- **sending a request from the north-bridge chip to South bridge chip** (lines 25-30 of column 3 mention that the system controller 114 transfers ROM data 102 to RAM 118. Thus, the North Bridge 114 requests for initialization data 102 through South Bridge 110) **in order to access initialization data from the non-volatile memory** (lines 20-35 of column 1);
- **in response to the request, accessing the second memory space of the non-volatile memory to read out initialization data by south bridge chip** (Fig 1 shows that the ROM data 102 is read and sent by 110);
- **sending the initialization data from the South bridge chip to the North Bridge chip** (Fig 1 shows the arrow from 104 to 116. Thus, the ROM data 102 is transferred from 104 to 116, which includes sending data from 110 to 114)
- **activating the central processor unit by receiving the initialization data sent from the south-bridge chip** (lines 7-12 of column 4 mention that CPU is activated after firmware transfers to RAM, which includes 114) **and then initializing the central processing unit based on the initialization data**

received by the north-bridge chip from the south bridge chip (lines 1-20 of column 2).

Klein (US Patent 6216224) does not explicitly mention that 114 is the north bridge and 110 is the south bridge. Instead, 114 is labeled as system controller in line 7 of column 2 and 110 is labeled as ISA-PCI bridge in line 28 of column 4.

System controller and ISA-PCI bridge are known as north bridge and south bridge respectively. To support the statement, Examiner presents Klein (US Patent 5974239), which mentions that system controller is sometimes called the north bridge (lines 47-48 of column 1) and the bridge between PCI and ISA bus is called South bridge (lines 60-61 of column 1; lines 59-60 of column 4). Thus, Klein (US Patent 5974239) interchangeably used “system controller” with “north bridge” and “ISA bridge” with “south bridge”.

Klein does not teach setting initial values for initialization of the CPU based on received initialization data received by North bridge. Klein uses a random access memory to store initialization data.

AAPA teaches setting initialization values for initialization using the initialization data sent by the north bridge (lines 20-27 of column 2). AAPA does not use any RAM to store initialization data (Fig 2).

It would have been obvious to one ordinary skill in the art at the time the invention was made to have combined the teachings of applicant's admission of prior art and Klein. One ordinary skill in the art would have been motivated to set initial values for initialization of the CPU based on received initialization data from North Bridge, since that is a necessary step for initialization. One ordinary skill in the art would be motivated to omit the RAM as it is a faster way to initialize the CPU.

For claim 13, Klein does not teach activating North bridge by South Bridge. AAPA teaches (note lines 19-21 of [0007] of page 3 of applicant's disclosure) that the South Bridge is powered and starts up the North Bridge. One ordinary skill would be motivated to start South Bridge first and then North bridge by sending signal from South Bridge, as it is one of the conventional system in the art.

For claim 14, note Fig 1 of applicant's disclosure.

For claim 15, 104 is the ROM containing BIOS.

For claim 16, the mentioned steps are required for transferring initialization data from non-volatile memory to system memory through South Bridge under the driving of North Bridge.

For claim 17, note lines 1-17 of column 2.

For claim 18, Klein mentions that the address counter preloads an initial address, which is the highest address for ROM data that is transferred from ROM to RAM in lines 30-35 of column 5. Thus, the ROM data contains an initialization ID.

For claim 19, Klein does not teach SIP data. AAPA teaches (lines 23-24 of page 2 of applicant's disclosure) that the initialization data may include SIP data used in AMD CPUs. One ordinary skill would be motivated to have initialization data to include SIP data, as it is useful for AMD CPUs.

For claim 20, Klein teaches the following limitations:

a system for accessing initialization data (102 in Fig 1) **for starting a central processor unit** (lines 55-57 of column 3; lines 5-10 of column 1), **the system comprising:**

- **a non-volatile memory including: a first memory space storing routines and BIOS and a second memory space storing initialization data, wherein the initialization data is excluded from the BIOS and is used for initialization of the CPU** (lines 28-36 of column 1 mention that firmware routines include BIOS and various initialization routines. Lines 55-60 of column 1 mention that BIOS firmware is different from initialization routines. Since BIOS and initialization routines are different, they are saved in different

space in firmware. Therefore, first memory space includes BIOS and second memory space includes initialization data);

- **a South Bridge chip** (110) **in direct communication with the non-volatile memory** (Fig 1), **the South Bridge chip, when requested for the initialization data, for accessing the initialization data from the second memory space of non-volatile memory** (Fig 1 shows that 102 is passed to 116 through 110. Thus, 110 accesses 102);
- **a system controller, or North Bridge chip** (114) **coupled between ISA-PCI bridge** (110) **and the central processor unit** (106), **the North Bridge chip, when activated, sends a request for initialization data to the South Bridge** (Fig 1);
- **wherein in response to the request from the system controller for obtaining the initialization data** (lines 27 of column 3 mention that the system controller is to transfer the ROM data to RAM. Thus, the North Bridge does the request to obtain ROM data from 104), **the ISA-PCI (i.e., South) bridge chip accesses the initialization data from the second memory space** (Fig 1) **and forwards the initialization data to the North bridge chip** (lines 1-5 of column 2) **for activating the central processor unit** (lines 1-20 of column 2).;
- **wherein in response to the initialization data sent from the South Bridge chip, the North Bridge chip activates the central processing unit based on the received initialization data from the South Bridge chip** (lines 5-13

of column 5 mention that RESET is deasserted and CPU is initialized after initialization routines are transferred from ROM to RAM. Therefore, CPU cannot be activated until initialization routines are transferred from ROM to RAM. Thus, based on receiving initialization routines from South bridge chip, north bridge 114 activates CPU).

Klein (US Patent 6216224) does not explicitly mention that 114 is the north bridge and 110 is the south bridge. Instead, 114 is labeled as system controller in line 7 of column 2 and 110 is labeled as ISA-PCI bridge in line 28 of column 4.

It is examiner's position that the system controller and ISA-PCI bridge are known as north bridge and south bridge respectively. To support the statement, Examiner presents Klein (US Patent 5974239), which mentions that system controller is sometimes called the north bridge (lines 47-48 of column 1) and the bridge between PCI and ISA bus is called South bridge (lines 60-61 of column 1; lines 59-60 of column 4). Thus, Klein (US Patent 6216224) interchangeably used "system controller" with "north bridge" and "ISA bridge" with "south bridge".

Klein does not teach setting initial values for initialization of the CPU based on received initialization data received by North bridge. Klein uses a random access memory to store initialization data.

AAPA teaches setting initialization values for initialization using the initialization data

sent by the north bridge (lines 20-27 of column 2). AAPA does not use any RAM to store initialization data (Fig 2).

It would have been obvious to one ordinary skill in the art at the time the invention was made to have combined the teachings of applicant's admission of prior art and Klein. One ordinary skill in the art would have been motivated to set initial values for initialization of the CPU based on received initialization data from North Bridge, since that is a necessary step for initialization. One ordinary skill in the art would be motivated to omit the RAM as it is a faster way to initialize the CPU.

For claim 21, Klein does not teach any power supply to activate South bridge. Fig 1 of applicant's disclosure show that South Bridge is connected to power supply controller. One ordinary skill in the art would be motivated to provide power to South Bridge as it is one of the accepted design in the art.

For claim 22, 104 is the ROM containing BIOS.

For claim 23, Klein mentions that the address counter preloads an initial address, which is the highest address for ROM data that is transferred from ROM to RAM in lines 30-35 of column 5. Thus, the ROM data contains an initialization ID.

For claim 24, Klein mentions that the address counter preloads an initial address, which is the highest address for ROM data that is transferred from ROM to RAM and the initial address may be provided by hardwiring in lines 30-50 of column 5. Thus, ROM includes a predetermined location for storing initialization data. Lines 50-55 of column 1 mention that after the CPU initialization is executed, it can be discarded and the RAM contains remaining BIOS. Thus, the initialization routines and BIOS have to be stored in separate area because they are separate routines.

For claim 25, Klein does not teach SIP data. AAPA teaches (lines 23-24 of page 2 of applicant's disclosure) that the initialization data may include SIP data used in AMD CPUs. One ordinary skill would be motivated to have initialization data to include SIP data, as it is useful for AMD CPUs.

For claim 26, Klein is retrieving the initialization data by the south bridge chip; and sending the initialization data to the north bridge chip.

However the south bridge chip of Klein does not include means for: activating the north bridge chip. Applicant's admission of prior art activates North Bridge by South Bridge.

It would have been obvious to one ordinary skill in the art to have combined the teachings of applicant's admission of prior art and Klein. One ordinary skill in the art would have been motivated to activate the North Bridge by South Bridge as disclosed in

applicant's admission of prior art, since South Bridge contains the initialization data, which should be started before other components.

For claim 27, lines 1-17 of column 2 mention that CPU reads initialization data.

Response to Arguments

Applicant's arguments filed on 2/9/07 with respect to claims 12, 15-17, 20, 22, 27 are moot in view of new grounds of rejections.

Applicant's arguments filed on 2/9/07 with respect to claims 1-6, 13-14, 18-19, 21, 23-26 have been fully considered but are not persuasive.

Applicant argues that combination of Klein and AAPA does not teach "no RAM to store initialization data". Examiner disagrees since AAPA does not use any RAM to store initialization data (Fig 2).

Applicant further argues that combination does not teach that "the initialization data is excluded from the BIOS and is used for initialization of the CPU".

Examiner disagrees. BIOS is clearly different from other initialization routines (lines 28-36 of column 1 mention that firmware routines include BIOS and various initialization

routines). These routines include CPU initialization routine (line 56 of column 1 mentions that the routine is CPU initialization routine).

Applicant further argues that there is no motivation to combine AAPA and Klein.

Examiner disagrees. Motivation for an ordinary skill is already provided in the action. Typically South bridge connects the non-volatile memory in the data processing system. Therefore, ordinary skill in the art would be motivated to place the non-volatile memory of AAPA connected to the South bridge. All other steps (ie, accessing South bridge by North bridge) are required for proper operation of the system, when non-volatile memory containing initialization data is placed on South bridge side (as shown in Klein).

Allowable Subject Matter

Claims 32-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A

shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

THUAN N. DU
PRIMARY EXAMINER